B. Amendments to the Claims

The following listing of the claims replaces all prior versions and listings of the claims in the application.

Claims 1-16 (Canceled)

17. (Currently Amended) A transistor formed on a substrate assembly, comprising:

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

a first pocket implant junction located in said substrate assembly ~~and~~, said first pocket implant junction comprising ~~an excess amount of dopant~~ a first high dose dopant implant and defining a first low-resistance path, wherein said first pocket implant junction is ~~characterized by a non-uniform dopant profile and extends under a first~~ in communication with a non-sidewall portion of said source and extends under a first portion of said gate;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of said gate oxide region in communication with at least a portion of said gate and said drain; and

a second pocket implant junction located in said substrate assembly ~~and~~, said second pocket implant junction comprising ~~an excess amount of dopant~~ a second high dose dopant implant and defining a second low-resistance path, wherein said second pocket implant junction is ~~characterized by a non-uniform dopant profile and extends under a first~~ in communication with a non-sidewall portion of said drain and extends under a second portion of said gate.

Claims 18-97 (Canceled)

98. (Previously Presented) The transistor of claim 17, wherein said raised source includes doped polysilicon.

99. (Previously Presented) The transistor of claim 17, wherein said raised drain includes doped polysilicon.

100. (Previously Presented) The transistor of claim 17, wherein said gate includes doped polysilicon.

101. (Previously Presented) The transistor of claim 17, wherein said source includes a plug.

102. (Previously Presented) The transistor of claim 101, wherein said plug includes an adhesive layer.

103. (Previously Presented) The transistor of claim 17, wherein said gate includes a gate terminal.

Claims 104-124 (Canceled)

125. (Currently Amended) A transistor formed on a substrate assembly, comprising:

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

a first pocket implant junction located in said substrate assembly ~~and~~, said first pocket implant junction comprising ~~an excess amount of dopant~~ a first high dose dopant implant and defining a first low-resistance path, wherein said first pocket implant junction is ~~characterized by a non-uniform dopant profile and extends under a first~~ in communication with a non-sidewall portion of said source and extends under a first portion of said gate;

a first outdiffusion area located in said substrate assembly and extending under ~~a second~~ at least a portion of said source;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of said gate oxide region in communication with at least a portion of said gate and said drain;

a second pocket implant junction located in said substrate assembly ~~and~~; said second pocket implant junction comprising ~~an excess amount of dopant~~ a second high dose dopant implant and defining a second low-resistance path, wherein said second pocket implant junction is ~~characterized by a non-uniform dopant profile and extends under a first~~ in communication with a non-sidewall portion of said drain and extends under a ~~first~~ second portion of said gate; and

a second outdiffusion area located in said substrate assembly and extending under ~~a second~~ at least a portion of said drain.

126. (Previously Presented) The transistor of claim 125, wherein said first and second pocket implant junctions include phosphorous.

Claim 127 (Canceled)

128. (Currently Amended) A transistor formed on a substrate assembly, comprising:

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of said gate oxide region in communication with at least a portion of said gate and said drain; and

a halo implant structure located in said substrate assembly ~~and~~, said structure comprising a first pocket implant junction and a second pocket implant junction, wherein said first pocket implant junction includes ~~an excess amount of dopant and~~ a first high dose dopant implant ~~extends~~ in communication with a non-sidewall portion of said source and extends under a first edge of ~~the~~ said gate, and wherein said second pocket implant junction includes ~~an excess amount of dopant and~~ a second high dose dopant implant ~~extends~~ in communication with a non-sidewall portion of said drain and extends under a second edge of ~~the~~ said gate~~, and wherein the first and second implant junctions are each characterized by a non-uniform dopant profile~~.